HS40J (Preliminary)

Encoder modules

SPI interface

Application

- BLDC / PMSM Motor Control
- Stepping Motor Closed-Loop Systems
- Robotics & Collaborative Robots
- Automated Equipment & Industrial Motion Control
- Precision Positioning & Actuator Feedback

Features

- True power-on battery-less multiturn counter
- Up to **46 turns** non-volatile magnetic turn tracking
- **±0.25° single-turn angle accuracy (with supplied magnet & spacer, within specified operating window)**
- High-speed **100 kSPS** update rate
- Compact, robust, contamination-resistant magnetic design
- Built-in diagnostics for safety-critical applications (UV/OV, GMR/AMR fault, CRC, ECC)
- SPI digital interface
- Clockwise (CW) turn count increment
- Compact size and easy mounting

Resolution

Single-turn: 12-bit(0.0879° resolution)
Multi-turn: 46 turns (0°~16,560°)

Electrical Specifications

Interface		SPI, maximum 10MHz
Supply voltage{1}		3.3V±10% (for Type 33) 5.0V±10% (for Type T)
Supply current (Max.)		40mA
Output voltage	"H"	>0.7 Vcc{2}
	"L"	<0.3 Vcc

{1} Ripple < 100mV$_{p-p}$
{2} SPI Logic Level follows Supply Voltage Vcc. For 5V supply, Logic High is 5V.)

Environmental Specifications

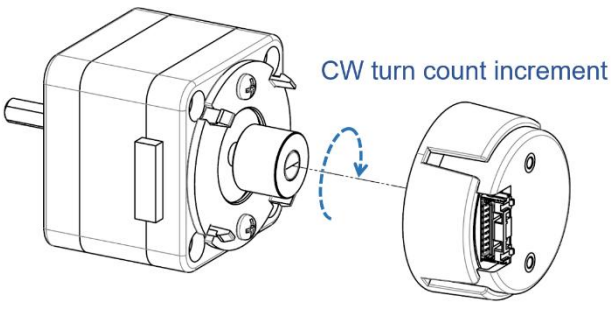
Operating Temp.	-40 ~ +125℃{4}
Storage Temp.	-40 ~ +125℃{4}
Operating Humidity	RH 85% Max. non-condensing
Shock	490 m/s^2, 3Dx2 times
Vibration	1.2mm,10~55Hz, 3Dx30min.
Protection	IP 40

{4} Except the wire and connector (-40 ~ + 80℃)

Mechanical Specifications

Blind bore diameter	Φ 5, 6, 6.35, 8mm
Housing material	PC
Max. R.P.M.{3}	28,000 rpm
Net Weight	20g

{3} PS. Dynamic phase lag due to system latency: error(°) = 8.64×10-4 × rpm



 Version 1.1 2026-03-03
info@honestsensor.com www.honestsensor.com

<Principle of Operation>

The HS40J encoder combines two magnetic sensing technologies to achieve true power-on multiturn position tracking. A **GMR-based turn sensor** monitors the movement of magnetic domain walls along a patterned nanowire structure. Each full rotation of the shaft's magnet causes a deterministic shift in the magnetic state, allowing the module to accumulate turn counts even when power is off.

For single-turn angle measurement, an **AMR vector sensor** detects the in-plane magnetic field and derives the shaft angle from the sine and cosine components of the field vector, providing high-resolution 360° position information. By fusing the GMR turn count with the AMR angle, the HS40J delivers a non-volatile, multiturn absolute position output. Proper mounting with the supplied magnet and spacer ensures the magnetic field stays within the specified operating window for guaranteed accuracy.

< Magnet & Mounting (Guaranteed Conditions)>

The HS40J is designed to operate with the **supplied magnet and precision spacer tool**, ensuring correct air-gap and alignment. The module requires the magnetic field to fall within its specified operating window, which is achieved only when the magnet is installed according to the defined fixture geometry. The air-gap and concentricity are controlled by the spacer tool and are not user-adjustable.

< Acceptance Test >

After the magnet and module are installed, an initial acceptance test is required to confirm proper mechanical alignment and magnetic strength. Power on the system and ensure that no diagnostic error is reported. Then verify that the measured magnetic-vector amplitude (RADIUS value) falls within the valid operating window. A correct RADIUS reading indicates that the air-gap, field strength, and magnet centering all meet the required conditions.
Acceptance criterion: RADIUS code must be within 4352 to 23296 (decimal) under normal installation.

If any diagnostic warning appears, or if the RADIUS value is outside the acceptable range, the magnet assembly must be reinstalled using the supplied spacer tool to restore the correct distance and alignment before the system is placed into service.

Caution (External magnetic field): The magnetic flux density at the HS40J shall not exceed **200 mT** (absolute maximum rating). Avoid strong stray magnetic fields from motors, brakes, magnetic fixtures, etc.

Important (Power-off rotation limit)
True power-on turn-count capability is guaranteed only within 0 to 46 turns. If the shaft is rotated beyond this range while the module is unpowered, the reported absolute angle can be incorrect after the next power-on and a FAULT flag may NOT be set. The system must include mechanical end-stops or an installation/service procedure to prevent rotation beyond 0 to 46 turns when power is OFF.

<GMR Turn-Count Reset Conditions & Methods>

A reset of the multiturn magnetic counter is required after initial assembly or whenever the module reports an invalid turn-state condition (e.g., FAULT bit D9 or D13). Typical causes include incorrect magnetic domain transitions or mismatch between the stored turn state and the measured angle.
The reset can be performed using either of the following methods:

1. Mechanical Reset:
   Rotate the shaft **46 full turns clockwise** to drive the magnetic-domain pattern back to its reference state.

2. Magnetic Reset(optional tooling):
   Apply an external magnetic field **> 60 mT** at an angle of approximately **315°**. For reliable and repeatable field orientation, an **optional HONEST SENSOR reset fixture/tooling** can be used.

After completing the reset process, **restart the encoder module** to resume normal operation.

Note: Magnetic reset is **not a zeroing operation**. After reset, the reported multi-turn value **depends on the shaft angle at the moment of reset** and may appear as **45 or 46 turns**. This is normal behavior.

SPI interface

SPI TIMING SPECIFICATIONS

Vcc = 3.3 V ±10% or 5 V ±10%, VSS = 0 V

Table 1. SPI Timing Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
f_{SCLK}			10	MHz	SCLK Frequency
t_{CSS}	0			ns	$\overline{CS}$ Setup Time
t_{CSH}	0			ns	$\overline{CS}$ Hold Time
t_{CSD}	0			µs	$\overline{CS}$ Disable Time
t_{SU}	20			ns	Data Setup Time
t_{HD}	20			ns	Data Hold Time
t_R	0		5	ns	SCLK Rise Time
t_F	0		5	ns	SCLK Fall Time
t_{HIGH}	40			ns	SCLK High Time
t_{LOW}	40			ns	SCLK Low Time
t_{CLD}	10			ns	SCLK Delay Time
t_{CLE}	10			ns	SCLK Enable Time
t_V			40	ns	Output Valid from SCLK Transfer Low
t_{HO}	10			ns	Output Hold Time
t_{DIS}			5	ns	Output Disable Time

SPI logic levels follow VIN (3.3 V or 5 V). Timing is referenced to the 50% VIN level.

SPI TIMING DIAGRAMS

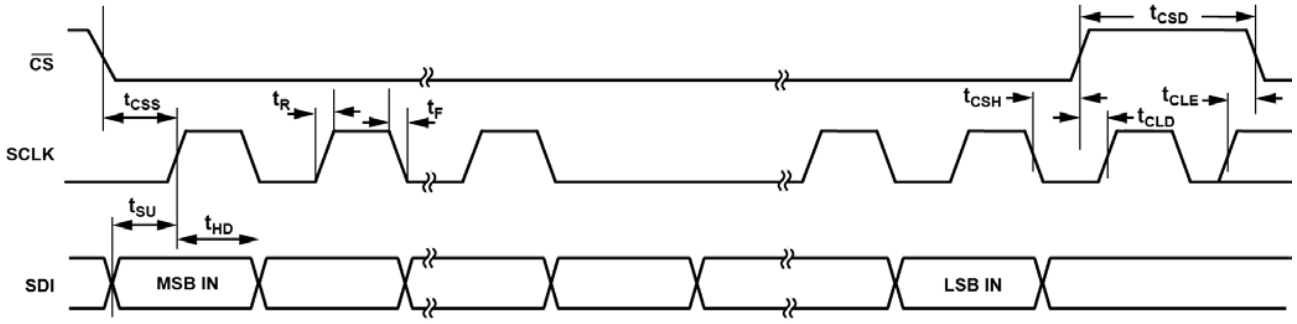


Figure 1. SPI Controller Request Timing Diagram

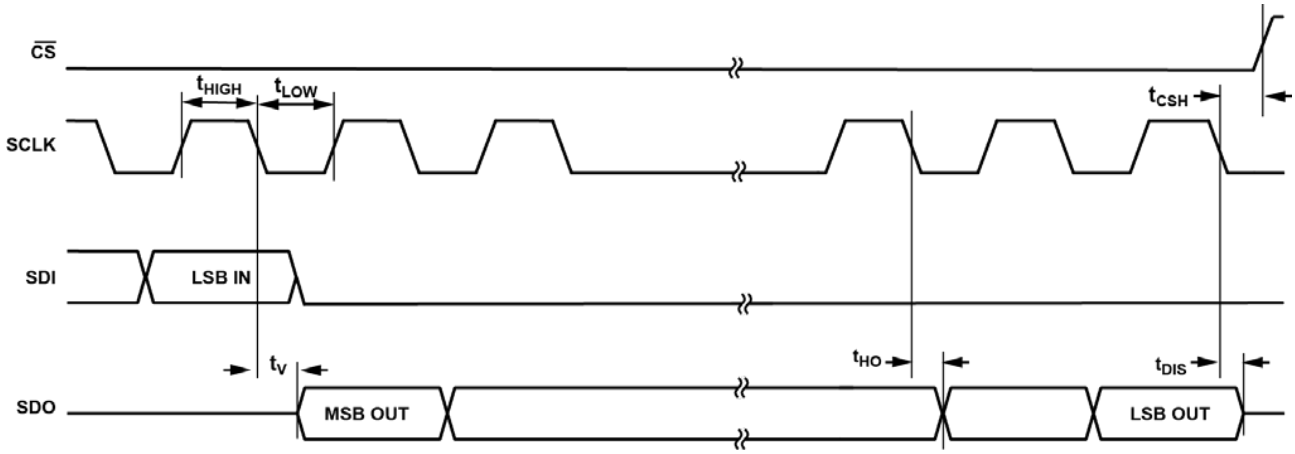


Figure 2. SPI timing diagram for Subordinate Response.

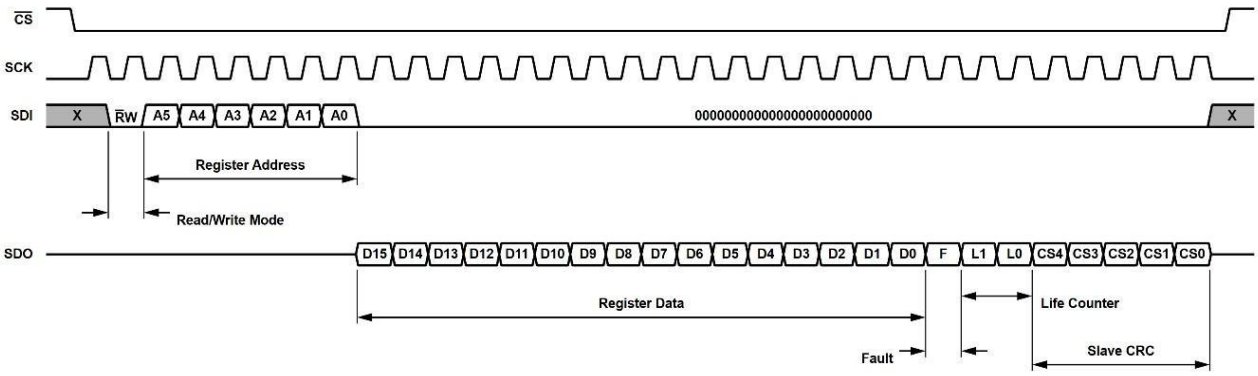


Figure 3. SPI register read operation

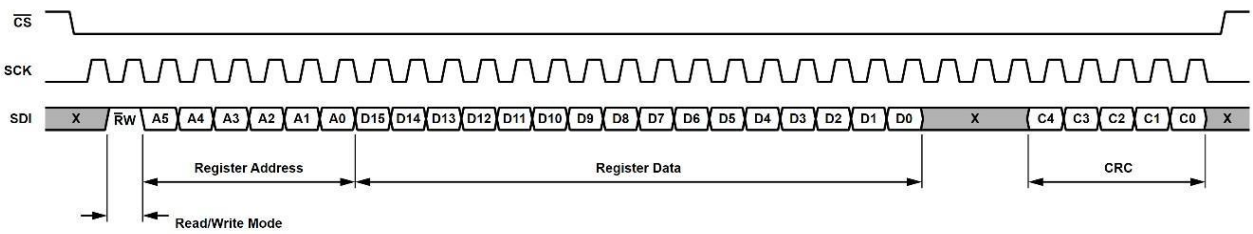


Figure 4. 32-bit write operation for 16-bit register

SPI Interface & Timing

- Mode: SPI Mode 0 (CPOL=0, CPHA=0), MSB-first
- Clock: $f^{SCLK} \leq 10$ MHz
- Frame: 32-bit read/write per 16-bit register. Multi-register burst is supported while $\overline{CS}$ is held low.

Transactions

Coherent position read (MANDATORY for synchronized data): Read ABSANGLE (0x03) and ANGLE (0x05) in one single SPI transaction while $\overline{CS}$ is held low (e.g., a 64-bit transaction built from two 32-bit read frames). Keeping $\overline{CS}$ low prevents the second register from being updated before it is read.

Position outputs:
- ABSANGLE (0x03) -> 16-bit multi-turn absolute position (0° to 16,560°)
  - Includes Turn Count (0~46 turns) and **Coarse** Intra-turn angle (10-bit, **0.35°** /LSB).
- ANGLE (0x05) -> 12-bit **High-Resolution** Single-turn angle (0° to 360°, **0.0879°** /LSB).

Diagnostics:
Read FAULT (0x06) at power-up (expect 0xFFFF), then clear to 0x0000 and poll periodically.

Fault Diagnostics Overview

The FAULT register (0x06) latches safety-relevant error flags. On power-up the value is 0xFFFF; the host must verify this pattern, then clear the register. A bit set to '1' can only be cleared after the root cause is removed. Key groups are
• Power-supply monitor (bits D0–D3)
• Memory integrity (D5, D7)
• Sensor plausibility checks – GMR status (D9, D13) and AMR radius check (D14). (ANGLE vs ANGLESEC plausibility is evaluated by the host.)
Continuous monitoring of these flags is essential for functional-safety applications.

Most registers are organised in pages. Write the desired page number into CNVPAGE[4:0] (address 0x01) before accessing a paged register. Page-agnostic primary registers—ABSANGLE, ANGLE, FAULT, and CNVPAGE—can be accessed without page switching.

Table 2. Operating Window & Supply Monitor Thresholds

Parameter	Conditions / Comment	Min	Typ	Max	Unit
Angle sensor radius		4352		23296	Code (decimal)
Power Supply					
V_{DD} Undervoltage			3.0		V
V_{DD} Overvoltage			5.4		V
V_{DRIVE} Undervoltage			1.5		V
V_{DRIVE} Overvoltage			5.7		V

Module Register Summary (for system integration)

HS40J provides position and diagnostics through the following primary registers:
- ABSANGLE (0x03, Read): 16-bit multi-turn absolute position (0° to 16,560°), with 10-bit intra-turn angle (0.3516°/LSB)
- ANGLE (0x05, Read): 12-bit single-turn angle (0° to 360°), 0.0879°/LSB
- FAULT (0x06, Read/Write): diagnostic flags (read 0xFFFF at power-up, then clear to 0x0000)

For advanced configuration and calibration registers, refer to Appendix A.

ABSANGLE Format & Interpretation

ABSANGLE (0x03) reports the absolute multi-turn position over 0° to 16,560° (0 to 46 turns).
- **[15:10]**: whole-turn count (0 to 46).
- **[9:8]**: quadrant (quarter-turn) information.
- **[9:0]**: intra-turn angle (10-bit), **0.3516°/LSB**.

If the turn count exceeds the valid range, **FAULT.D13** is asserted.

Primary vs Secondary Angle

ANGLE (0x05) contains the fully-corrected primary angle. ANGLESEC (0x08) provides an independently-derived secondary angle for plausibility checking. The host should periodically compare ANGLE and ANGLESEC within a sufficiently short time interval and take appropriate action if the deviation exceeds the application-defined threshold. (Note: FAULT.D10 is reserved/not active.)

• Connection

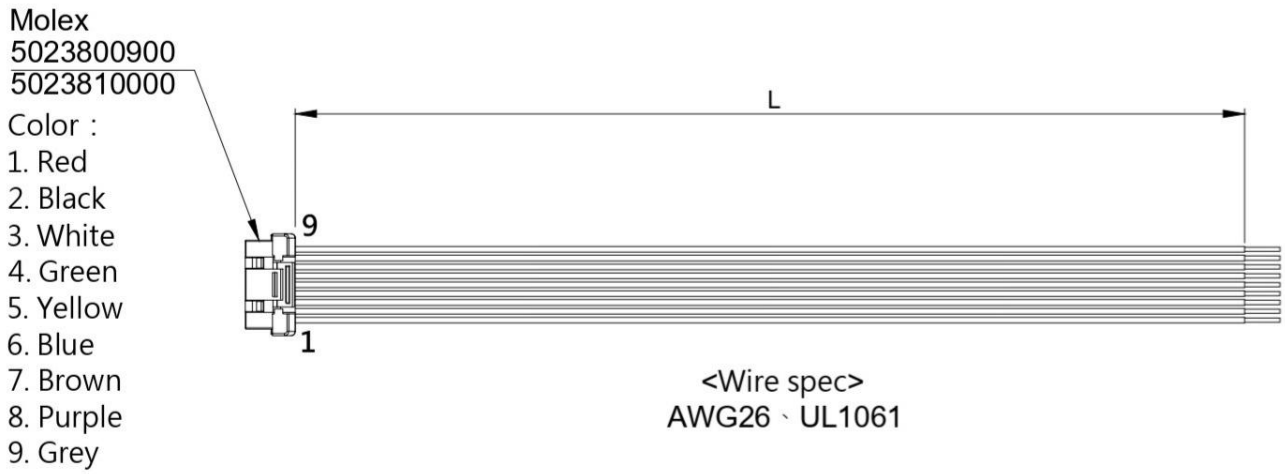
<SPI>

Signal : (UL1061、AWG26、9 wire)

Molex-5023860970

Red	Black	White	Green	Yellow	Blue	Brown	Purple	Grey
Vcc	Gnd	SCLK	SDI	SDO	$\overline{CS}$	BUSY	$\overline{CNV}$	ACALC

• Wire Introduction



Wire length：200mm

• Ordering Information

HS40J - AM - 12S - 46T - X SP X - X - NXXX

Encoder type	
AM	Absolute module

Single-turn resolution	
12S	12 bit

Multi-turn resolution	
46T	46 turn

Shaft diameter	
5	5mm
6	6mm
6.35	6.35mm
8	8mm

Output interface	
SP	SPI Interface

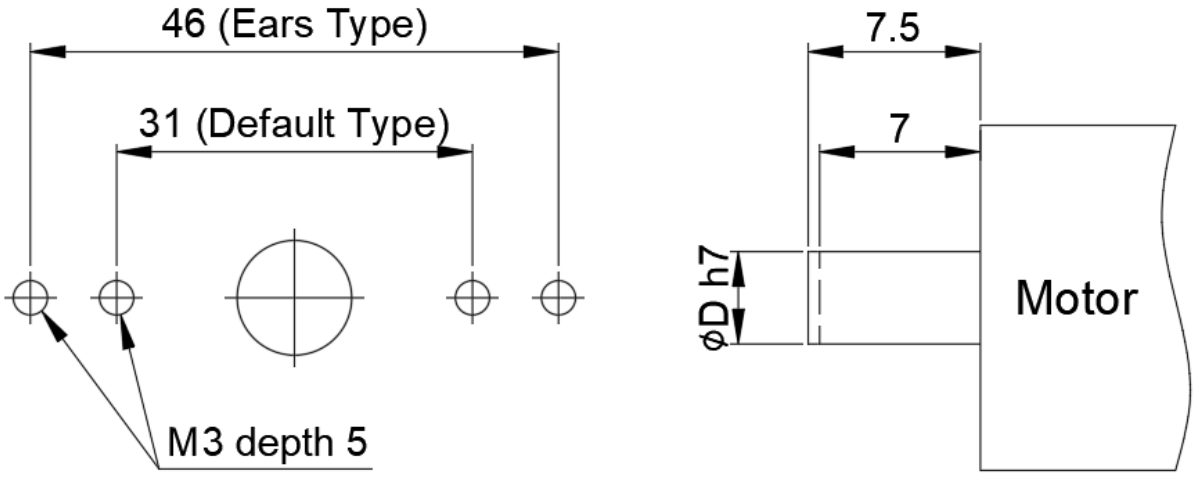
Supply voltage	
T	DC 5V
33	DC 3.3V

Base	
D	default
E	ears

Customized No.
001, 002, 003 …

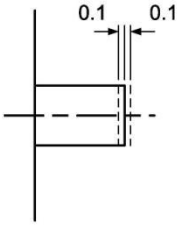
• Setting Dimension

Mounting Screw Size：M3 x 5mm

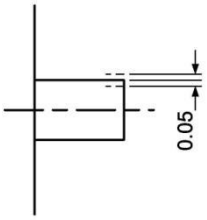


Mounting screw size：M3x5 mm　　Unit：mm

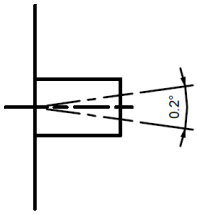
Axial assembly tolerance



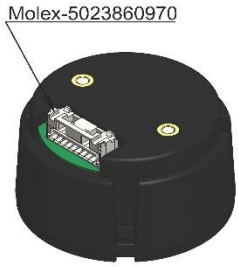
Radial assembly tolerance



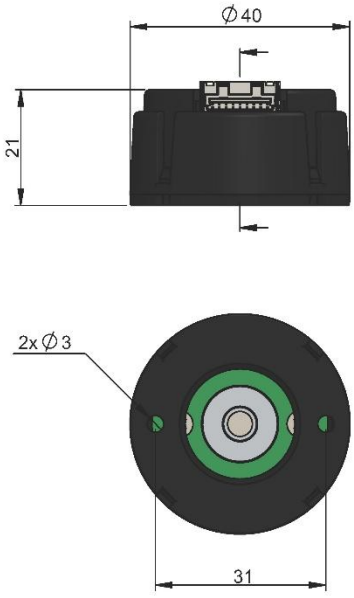
Concentric angle tolerance

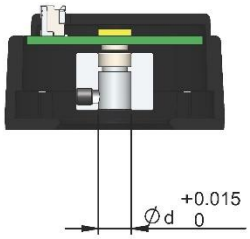


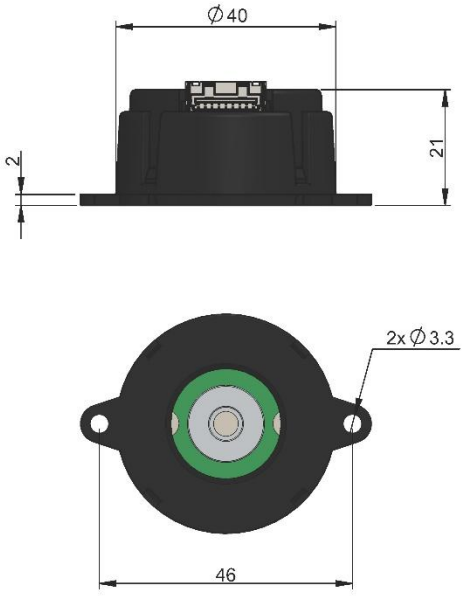
- **Mechanical Drawing**



<SPI>







Default Type

Ear Type

Appendix A - Advanced Register Descriptions

This appendix contains detailed register maps and bit descriptions for advanced configuration and calibration. Typical system integration only needs the primary registers listed in the main body.

REGISTER DETAIL

The register map for the HS40J is split into pages. To access registers on a specific page, the appropriate page address must be written into the CNVPAGE register. The default (power-on-reset) value for each register is 0x0000, unless otherwise stated in Table 3. The CNVPAGE, ABSANGLE, DIGIO, ANGLE, and FAULT registers are page agnostic, which means that they can be accessed without setting the CNVPAGE register before they are addressed.

Table3. Register map summary

Register	Function	Page	Address	Default Value	Access
CNVPAGE	Convert Start and Page Select	Agnostic	0x01	0x0000	R/W
ABSANGLE	Absolute Angle	Agnostic	0x03	0xDB00	R
DIGIO	Digital Input Output	Agnostic	0x04	0x0000	R/W
ANGLE	Angle Register	Agnostic	0x05	0x8000	R
FAULT	Fault Register	Agnostic	0x06	0xFFFF	R/W
SINE	Sine Measurement	0x00	0x10	0x0000	R
COSINE	Cosine Measurement	0x00	0x11	0x0000	R
RADIUS	Angle Measurement Radius	0x00	0x18	0x0000	R
TMP	Temperature Sensor	0x00	0x20	0x0000	R
GENERAL	General Device Configuration	0x02	0x10	0x1230	R/W
DIGIOEN	Enable Digital Input/Outputs	0x02	0x12	0x201F	R/W
CNVCNT	Conversion Count	0x02	0x14	0x0000	R
H1MAG	1st harmonic Error Magnitude	0x02	0x15	0x0000	R/W
H1PH	1st Harmonic Error Phase	0x02	0x16	0x0000	R/W
H2MAG	2nd Harmonic Error Magnitude	0x02	0x17	0x0000	R/W
H2PH	2nd Harmonic Error Phase	0x02	0x18	0x0000	R/W

H3MAG	3rd Harmonic Error Magnitude	0x02	0x19	0x0000	R/W
H3PH	3rd Harmonic Error Phase	0x02	0x1A	0x0000	R/W
H8MAG	8th Harmonic Error Magnitude	0x02	0x1B	0x0000	R/W
H8PH	8th Harmonic Error Phase	0x02	0x1C	0x0000	R/W
ECCEDC	Error Correction and Detection Codes	0x02	0x1D	0xXXXX	R/W
UNIQID0	Unique ID Register 0	0x02	0x1E	0xXXXX	R
UNIQID1	Unique ID Register 1	0x02	0x1F	0xXXXX	R
UNIQID2	Unique ID Register 2	0x02	0x20	0xXXXX	R
UNIQID3	Product, Voltage Supply, and ASIC Revision	0x02	0x21	0x0002	R
ECCDIS	Error Correction Code Disable	0x02	0x23	0x0000	R/W

Critical Configuration Registers

ABSANGLE Format & Interpretation

Refer to the ABSANGLE description in the main text (Module Register Summary section). No additional format differences apply.

Primary vs Secondary Angle

ANGLE (0x05) contains the fully-corrected primary angle. ANGLESEC (0x08) provides an independently-derived secondary angle for plausibility checking. The host should periodically compare ANGLE and ANGLESEC within a sufficiently short time interval and take appropriate action if the deviation exceeds the application-defined threshold. (Note: FAULT.D10 is reserved/not active.)

Page Agnostic Registers

$\overline{\text{CNV}}$ and Register Page Select

Address: 0x01, Reset: 0x0000, Name: CNVPAGE
The CNVPAGE register has two functions:
1. Select the page of the register that the user wants to access. If accessing multiple registers on the same page the CNVPAGE register need only be set before the first register access.

2. Trigger or abort a conversion sequence, setting the upper two bits of the CNVPAGE register to 0b00 will start a conversion sequence, setting 0b11 will abort a conversion sequence Table 4.

Table4. Bit descriptions for the CNVPAGE register.

Bits	Bit Name	Description	Access
[15:14]	$\overline{\text{CNV}}$	00 mimics the falling edge of convert start pin to trigger conversions. 11 mimics the rising edge of convert start pin to abort a conversion.	R/W
[13:5]	RESERVED	Reserved.	R
[4:0]	PAGE	Register Page Address.	R/W

Absolute Angle Register

Address: 0x03, Reset: 0xDB00, Name: ABSANGLE

The ABSANGLE register stores the combined turn count and angle information with a range of 16560°.

ABSANGLE [15:8] contains the turn count in quarter turns.

The upper six bits contain the number of whole turns, including a code for an invalid turn count:

- 0b0000 00 to 0b1101 01: straight binary turn count.
- 0b1101 10: invalid turn count.
- 0b1101 11 to 0b1111 11: two's compliment turn count value.

The lower ten bits contain the angle information in straight binary with a resolution of 0.351°.

Table5. Bit description for the ABSANGLE register.

Bits	Bit Name	Description	Access
[15:0]	ABSANGLE	Absolute angle	R

Digital Input Output Register

Address: 0x04, Reset: 0x0000, Name: DIGIO

Depending on how the GPIO ports are configured with the DIGIOEN register, the DIGIO register is used to either set or read the state of GPIO ports. The GPIO pins are mapped directly to the bit position in the register, GPIO5 to GPIO0 are controlled by DIGIO[5:0] respectively.

Table 6. Bits descriptions for the DIGIO register.

Bits	Bit Name	Description	Access
[15:6]	RESERVED	Reserved	R
[5:0]	DIGIO	GPIO logic state	R/W

Angle Register

Address: 0x05, Reset: 0x8000, Name: ANGLE

This register stores the angle information with the offset, gain, phase, and harmonic corrections applied and provides an accurate 0° to 360° position. See the

Sequencer section for details on when the angle register is updated.
Angle Resolution = 360°/4096.

Table 7. Bit descriptions for the ANGLE register.

Bits	Bit Name	Description	Access
[15:4]	ANGLE	Magnetic field angle with 360° range.	**R**
[3:0]	RESERVED	Reserved	**R**

Fault Register

Address: 0x06, Reset: 0xFFFF, Name: FAULT
The FAULT register stores various fault flags. Following a power- on reset, the FAULT register is set to 0xFFFF. The user should verify that all bits can be set to 0xFFFF by reading this register at power up. After verifying the register functionality, the user should clear the register to 0x0000. A bit in the FAULT register will stay set to high until the user writes a zero to that bit, the fault bit will not clear if the condition persists.

Table 8. Bit descriptions for the FAULT register.

Bits	Function	Description	Status	Access
D15	RESERVED	Reserved.	Not Active	R/W
D14	AMR Angle Sensor Radius Check	AMR Angle Sensor Radius Check.	Active	R/W
D13	Turn Counters Cross-Check Error	D13 bit flags if any of the following are detected: • The difference between turn count reported in the ABSANGLE register and the GMR turn count sensor exceeds 0.5 turns. • The turn count is above 46.5 turns or below 0 turns while the part is powered up. • The primary and redundant turn count decoders do not match. • There is a GMR turn count sensor and AMR angle sensor combination logic error. • A GMR quadrant sensor decode error occurs.	Active	R/W
D12	RESERVED	Reserved.	Not Active	R/W
D11	RESERVED	Reserved.	Not Active	R/W
D10	RESERVED	Reserved.	Not Active	R/W
D9	GMR Turn Count Sensor False State or Reference Resistor Flip	D9 flags if any of the following are detected: • An unrecognized state of the GMR turn count sensor, • A reference resistor in the wrong state, • An illegal value (either 0x01 or 0b10) is set in the, CW/CCW NVM setting, • The turn count is between 0 turns to typically 2 turns.	Active	R/W
D8	RESERVED	Reserved.	Not Active	R/W
D7	ECC Double Bit Error	Two-bit fault detected in NVM or user-configuration registers.	Active	R/W
D6	RESERVED	Reserved.	Not Active	R/W
D5	NVM CRC Fault	Nonvolatile memory CRC fault.	Active	R/W

D4	RESERVED	Reserved.	Not Active	R/W
D3	VDRIVE Overvoltage Detected	VDRIVE above the expected range, see Table 2.	Active	R/W
D2	VDRIVE Undervoltage Detected	VDRIVE below the expected range, see Table 2.	Active	R/W
D1	VDD Overvoltage Detected	VDD above the expected range, see Table 2.	Active	R/W
D0	VDD Undervoltage Detected	VDD below the expected range, see Table 2.	Active	R/W

Secondary Angle Register

Address: 0x08, Reset: 0x8000, Name: ANGLESEC

The Secondary Angle is a diagnostic feature which verifies the signal path of the primary angle (ANGLE). ANGLESEC is calculated using alternate combinations of the half-bridges from the AMR angle sensor and updated as per the sequencer mode.

The Secondary Angle is calculated from the SECANGLI and SECANGLEQ after the AMR sensor offset correction has been applied. AMR sensor offset TC and harmonic correction are not applied to the Secondary Angle.

The STATUS bit of the ANGLESEC register is set high when the register has new data. Once the register has been read on the SPI interface the STATUS bit will be set low to indicate that the data has already been accessed by the user. In One-Shot Mode the STATUS bit will always be set low, ANGLESEC is calculated at the end of the one shot sequence and so the ANGLE and ANGLESEC data can be compared once the full conversion sequence is complete. The ANGLESEC value is updated at ~1.2ms rate so in a rotating magnetic field it should be checked against the ANGLE data within a sufficiently short time interval.

Angle resolution = 360°/4096

Table 9. Bit description for the ANGLESEC register.

Bits	Bit Name	Description	Access
[15:4]	ANGLESEC	Secondary magnetic field angle measurement with 360° range	R
[3:1]	RESERVED	Reserved	
[0]	STATUS	Set to one for new data	R

Page 0x0 Registers

Sine Register

Page: 0x00, Address: 0x10, Reset: 0x0000, Name: SINE

The SINE register contains the value of the sine portion of the AMR angle sensor without the sensor gain, offset and harmonic calibration applied.

At the start of a measurement sequence, the register is set to 0x2000 and is updated once a valid measurement is available. The reset value of the register is 0x0000 and is stored in 2's complement data format.

Table 10. Bit descriptions for the SINE register.

Bits	Bit Name	Description	Access
[15:2]	SINE	Uncorrected sine output	R
[1]	RESERVED	Reserved	R
[0]	STATUS	During continuous conversions this flag is set high when new data is available. This flag is set low when the user reads the register contents. In One Shot mode this bit is always set low.	R

Cosine Register

Page: 0x00, Address: 0x11, Reset: 0x0000, Name: COSINE
The COSINE register contains the value of the cosine portion of the AMR angle sensor without the sensor gain, offset and harmonic calibration applied. At the start of a measurement sequence, the register is set to 0x2000 and is updated once a valid measurement is available. The reset value of the register is 0x0000 and is stored in 2's complement data format.

Table 11. Bit descriptions for the COSINE register.

Bits	Bit Name	Description	Access
[15:2]	COSINE	Uncorrected cosine output	R
[1]	RESERVED	Reserved	R
[0]	STATUS	During continuous conversions this flag is set high when new data is available. This flag is set low when the user reads the register contents. In One Shot mode this bit is always set low.	R

In Phase Secondary Angle

Page: 0x00, Address: 0x12, Reset: 0x0000, Name: SECANGLI This register stores the uncorrected in-phase secondary
angle measurement which can be used for diagnostics (COSn - SINn). This register is updated every time a secondary angle measurement is performed in the sequencer Mode 2. At the start of a conversion sequence, the register is set to 0x8000 and the value is stored in 2's complement data format.

Table 12. Bit description for the SECANGLI register.

Bits	Bit Name	Description	Access
[15:2]	SECANGLI	Uncorrected in-phase secondary angle measurement	R
[1]	RESERVED	Reserved	R

info@honestsensor.com www.honestsensor.com

[0]	STATUS	During continuous conversions this flag is set high when new data is available. This flag is set low when the user reads the register contents. In One Shot mode this bit is always set low.	R

Quadrature Phase Secondary Angle

Page: 0x00, Address: 0x13, Reset: 0x0000, Name: SECANGLQ

This register stores the uncorrected quadrature-phase secondary angle measurement which can be used for diagnostics, COSn - SINp. This register is updated every time a secondary angle measurement is performed in sequencer Mode 2. At the start of a conversion sequence, the register is set to 0x8000 and the value is stored in 2's complement data format.

Table 13. Bit description for the SECANGLQ register.

Bits	Bit Name	Description	Access
[15:2]	SECANGLQ	Uncorrected quadrature- phase secondary angle measurement	R
[1]	RESERVED	Reserved	R
[0]	STATUS	During continuous conversions this flag is set high when new data is available. This flag is set low when the user reads the register contents. In One Shot mode this bit is always set low.	R

Radius

Page: 0x00, Address: 0x18, Reset: 0x0000, Name: RADIUS

This register stores the magnitude of the vector from the SINE and COSINE angle measurements in bits 15 to 1, the RADIUS. This parameter can be used to confirm that the field strength on the AMR angle sensor is above a minimum level determined by the user.

Resolution = 0.000924 mV/V.

Table 14. Bit description for the RADIUS register.

Bits	Bit Name	Description	Access
[15:1]	RADIUS	Angle vector magnitude, or radius.	R
[0]	STATUS	During continuous conversions this flag is set high when new data is available. This flag is set low when the user reads the register contents. In One Shot mode this bit is always set low.	R

Diagnostic Register 1

Page: 0x00, Address: 0x1D, Reset: 0x0000, Name: DIAG1

- DIAG1[15:8], MTDIAG1, stores the state of the eight GMR turn count sensor reference resistors used.
- DIAG1[7:0], AFEDIAG2 stores the result of a conversion of a fixed value voltage to

the GMR turn count sensor AFE, AFEDIAG2 used to verify the analog font end. AFEDIAG2 is stored in 2's complement data format where the resolution = 4.8828mV for a 5V part and 3.222mV for a 3.3V part.

- 0x80 represents -625mV and 0x7F represents 625mV for a 5V part, and
- 0x80 represents -412.5mV and 0x7F represents 412.5mV for a 3.3V part.

DIAG1 is set to 0x3380 at the start of every conversion sequence.

Table 15. Bit descriptions for the DIAG1 register.

Bits	Bit Name	Description	Access
[15:8]	MTDIAG1	State of eight diagnostic resistors	R
[7:0]	AFEDIAG2	Measurement of fixed voltage	R

Diagnostic Register 2

Page: 0x00, Address: 0x1E, Reset: 0x0000, Name: DIAG2 Diagnostic resistor values.

The HS40J has two diagnostic resistors set to +57% and -57% of the ADC range. The upper byte of this register stores the ADC result for the +57% diagnostic resistor channel while the lower byte stores the ADC result for the -57% diagnostic resistor channel. Measurements are stored in 2's complement format where the resolution = 0.78125%. 0x80 represents -100% and 0x7F represents 100%.

Table 16. Bit descriptions for the DIAG2 register.

Bits	Bit Name	Description	Access
[15:8]	AFEDIAG1	Measurement of AFE +57% diagnostic resistor	R
[7:0]	AFEDIAG0	Measurement of AFE -57% diagnostic resistor	R

Primary Temperature Sensor

Page: 0x00, Address: 0x20, Reset: 0x0000, Name: TMP0

This register stores the primary temperature sensor used for the AMR angle sensor calibration. This register is set to 0xFFF0 at the start of every conversion sequence.

For VDD = 5V

$TMP0^{DEGC} = (TMP0^{CODE} - 1145)/16.27$ For VDD = 3.3

$TMP0^{DEGC} = (TMP0^{CODE} - 1150)/16.32$

Where, $TMP0^{CODE}$ is the 12 bit register value and $TMP0^{DEGC}$ is the internal temperature in degrees Celsius.

Table 17. Bit description for the TMP0 register.

Bits	Bit Name	Description	Access
[15:4]	TMP0	Internal temperature sensor	R
[3:0]	RESERVED	reserved	R

Secondary Temperature Sensor

Page: 0x00, Address: 0x23, Reset: 0x0000, Name: TMP1

This register stores the secondary temperature sensor used to cross check the primary temperature sensor TMP0. This register is set to 0xFFF0 at the start of every conversion sequence.

For VDD = 5V
$TMP1^{DEGC} = (TMP1^{CODE} - 1238)/13.45$ For VDD = 3.3
$TMP1^{DEGC} = (TMP1^{CODE} - 1208)/13.61$
Where, $TMP1^{CODE}$ is the 12 bit register value and $TMP1^{DEGC}$ is the internal temperature in degrees Celsius.

Table 18. Bit description for the TMP1 register.

Bits	Bit Name	Description	Access
[15:4]	TMP1	Internal temperature sensor	R
[3:0]	RESERVED	reserved	R

Page 0x2 Registers

General Register

Page: 0x02, Address: 0x10, Reset: 0x1200, Name: GENERAL
This register enables control of various functions of the HS40J.
For ASIL B parts, the GENERAL register is set to 0x1200 by default, this configures the part as follows,

- Convert Start Synchronization mode off
- Angle Filter enabled
- Factory set eighth harmonic calibration coefficients
- Sequencer Mode 2
- Continuous
- conversion mode
- STORAGE[0:7] set to 0x00

The GENERAL register for Industrial and ASIL QM parts will be configured for sequence Mode 1 by default, 0x1230.

Table 19. Bit descriptions for the GENERAL register.

Bits	Bit Name	Description	Access
[15]	STORAGE[7]	Available for user data storage and part of ECC calculation.	R/W
[14:13]	CNVSYNC	Convert start synchronization mode 00: Sequencer controls the start of the sampling of the SINE and COSINE channels. 01: Not valid 11: Synchronize sampling instants of SINE and COSINE channels to convert start edge 10: Not valid	R/W
[12]	ANGLFILT	Filter on calculated angle 0: Filter disabled 1: Filter enabled	R/W
[11]	STORAGE[6]	Available for user data storage and part of ECC calculation.	R/W

[10]	H8CNTRL	8th Harmonic correction source 0: ADI factory-set values 1: User-supplied values	R/W
[9]	Reserved	This bit should be set 1.	R/W
[8:6]	STORAGE[5:3]	Available for user data storage and part of ECC calculation.	R/W
[5:4]	SEQNCR	Sequencer mode 00: Mode 2 01: Reserved 10: Reserved 11: Mode 1	R/W
[3:1]	STORAGE[2:0]	Available for user data storage and part of ECC calculation.	R/W
[0]	CNVMDE	Conversion Mode 0: Continuous conversions 1: One shot conversion, sequencer stops at the end of the conversion sequence	R/W

Digital Input/Output Enable Register

Page: 0x02, Address: 0x12, Reset: 0x241B, Name: DIGIOEN

All digital Input/Outputs can be used either in functional mode or GPIO mode. The relevant digital Input/Output pin can be configured as GPIO by setting the corresponding bit in the lower byte of this register high.

To enable the output drivers of the digital Input/Output pins, the bit for the corresponding pin should be set high. When the driver enable bit is set low and the function is set to GPIO the pin is configured as an input.

By default, DIGIOEN is configured to enable the BOOLOAD outputs at power on.

Table 20. Bit descriptions for the DIGIOEN register.

Bits	Bit Name	Description	Access
[15:14]	RESERVED	Reserved	R
[13]	DIGIO5EN	1: GPIO5 output enable 0: GPIO5 output disable	R/W
[12]	DIGIO4EN	1: GPIO4 output enable 0: GPIO4 output disable	R/W
[11]	DIGIO3EN	1: GPIO3 output enable 0: GPIO3 output disable	R/W
[10]	DIGIO2EN	1: GPIO2 output enable 0: GPIO2 output disable	R/W
[9]	DIGIO1EN	1: GPIO1 output enable 0: GPIO1 output disable	R/W
[8]	DIGIO0EN	1: GPIO0 output enable 0: GPIO0 output disable	R/W
[7:6]	RESERVED	Reserved	R
[5]	DIGIO5FNC	1: GPIO5	R/W
[4]	DIGIO4FNC	1: GPIO4 0: FAULT (output only)	R/W
[3]	DIGIO3FNC	1: GPIO3 0: ACALC (output only)	R/W
[2]	DIGIO2FNC	1: GPIO2	R/W

info@honestsensor.com www.honestsensor.com

[1]	DIGIO1FNC	1: GPIO1 0: $\overline{\text{CNV}}$ (input only)	R/W
[0]	DIGIO0FNC	1: GPIO0 0: BUSY (output only)	R/W

Angle Check

Page: 0x02, Address: 0x13, Reset: 0x000F, Name: ANGLECK

This register stores the threshold/limit for the primary angle versus secondary angle comparison. and is loaded during boot. The default value of 0x00F will be loaded during the power up sequence which sets the threshold limit to 5°. The user can modify the threshold limit to suit the application requirements. Resolution is 180°/1024 = 0.17578125°.

0x000 : will always generate a fault flag

0x001 through 0x200 : valid limits

0x201 through 0x3FF : will disable this check

Table 21. Bit descriptions for the ANGLECK register.

Bits	Bit Name	Description	Access
[15:10]	RESERVED	Reserved	R
[9:0]	ANGLECK	Conversion counter	R/W

Conversion Count Register

Page: 0x02, Address: 0x14, Reset: 0x0000, Name: CNVCNT

This register stores the conversion count information and is updated every time a conversion sequence is completed. The conversion counter doesn't increment if the conversion sequence is aborted early by initiating a new conversion sequence whilst the current conversion sequence is executing. On reaching the full scale value of 0xFF the counter wraps around to 0x00.

Table 22. Bit descriptions for the CNVCNT register

Bits	Bit Name	Description	Access
[15:8]	RESERVED	Reserved	R
[7:0]	CNVCNT	Conversion counter	R/W

1st Harmonic Error Calibration Magnitude

Page: 0x02, Address: 0x15, Reset: 0x0000, Name: H1MAG

This register stores the amplitude of the 1st harmonic error. The user should multiply the calculated harmonic coefficient by the CORDIC scaler of 0.6072 and write the resulting unsigned integer to the register. The LSB is 11.2455°/2^{11} = 0.005493°.

Table 23. Bit Descriptions for the H1MAG register.

Bits	Bit Name	Description	Access
[15:11]	RESERVED	Reserved	R
[10:0]	H1MAG	1st harmonic error amplitude	R/W

1st Harmonic Error Calibration Phase

Page: 0x02, Address: 0x16, Reset: 0x0000, Name: H1PH

This register stores the phase of the 1st harmonic error as an unsigned integer with an LSB of $360°/2^{12} = 0.087891°$.

Table 24. Bit descriptions for the H1PH register.

Bits	Bit Name	Description	Access
[15:12]	RESERVED	Reserved	R
[11:0]	H1PH	1st harmonic error phase	R/W

2nd Harmonic Error Calibration Magnitude

Page: 0x02, Address: 0x17, Reset: 0x0000, Name: H2MAG

This register stores the amplitude of the 2nd harmonic error. The user should multiply the calculated harmonic coefficient by the CORDIC scaler of 0.6072 and write the resulting unsigned integer to the register. The LSB is $11.2455°/2^{11} = 0.005493°$.

Table 25. Bit descriptions for the H2MAG register·

Bits	Bit Name	Description	Access
[15:11]	RESERVED	Reserved	R
[10:0]	H2MAG	2nd harmonic error amplitude	R/W

2nd Harmonic Error Calibration Phase

Page: 0x02, Address: 0x18, Reset: 0x0000, Name: H2PH

This register stores the phase of the 2nd harmonic error as an unsigned integer with an LSB of $360°/2^{12} = 0.087891°$.

Table 26. Bit Descriptions for the H2PH register.

Bits	Bit Name	Description	Access
[15:12]	RESERVED	Reserved	R
[11:0]	H2PH	2nd harmonic error phase	R/W

3rd Harmonic Error Calibration Magnitude

Page: 0x02, Address: 0x19, Reset: 0x0000, Name: H3MAG

This register stores the amplitude of the 3rd harmonic error. The user should multiply the calculated harmonic coefficient by the CORDIC scaler of 0.6072 and write the resulting unsigned integer to the register. The LSB is $1.40076°/2^{8} = 0.005493°$.

Table 27. Bit descriptions for the H3MAG register.

Bits	Bit Name	Description	Access
[15:8]	RESERVED	Reserved	R
[7:0]	H3MAG	3rd harmonic error amplitude	R/W

info@honestsensor.com www.honestsensor.com

3rd Harmonic Error Calibration Phase

Page: 0x02, Address: 0x1A, Reset: 0x0000, Name: H3PH

This register stores the phase of the 3rd harmonic error as an unsigned integer with an LSB of $360°/2^{12} = 0.087891°$.

Table 28. Bit descriptions for the H3PH register.

Bits	Bit Name	Description	Access
[15:12]	RESERVED	Reserved	R
[11:0]	H3PH	3rd harmonic error phase	R/W

8th Harmonic Error Calibration Magnitude

Page: 0x02, Address: 0x1B, Reset: 0x0000, Name: H8MAG

This register stores the amplitude of the 8th harmonic error. The user should multiply the calculated harmonic coefficient by the CORDIC scaler of 0.6072 and write the resulting unsigned integer to the register. The LSB is $1.40076°/2^{8} = 0.005493°$.

Table 29. Bit descriptions for the H8MAG register.

Bits	Bit Name	Description	Access
[15:8]	RESERVED	Reserved	R
[7:0]	H8MAG	8th harmonic error amplitude	R/W

8th Harmonic Error Calibration Phase

Page: 0x02, Address: 0x1C, Reset: 0x0000, Name: H8PH

This register stores the phase of the 8th harmonic error as an unsigned integer with an LSB of $360°/2^{12} = 0.087891°$.

Table 30. Bit descriptions for the H8PH register.

Bits	Bit Name	Description	Access
[15:12]	RESERVED	Reserved	R
[11:0]	H8PH	8th harmonic error phase	R/W

Unique ID Register 0

Page: 0x02, Address: 0x1E, Reset: 0xXXXX, Name: UNIQID0 Unique identification register 0.

Table 32. Bit descriptions for the UNIQID0 register.

Bits	Bit Name	Description	Access
[15]	RESERVED	Reserved	R
[14:0]	UNIQID0	Unique device identification 0	R

Unique ID Register 1

Page: 0x02, Address: 0x1F, Reset: 0xXXXX, Name: UNIQID1 Unique identification register 1.

Table 33. Bit descriptions for the UNIQID1 register.

Bits	Bit Name	Description	Access
[15:0]	UNIQID1	Unique device identification 1	R

Unique ID Register 2

Page: 0x02, Address: 0x20, Reset: 0xXXXX, Name: UNIQID2 Unique identification register 2.

Unique ID Register 3

Page: 0x02, Address: 0x21, Reset: 0xXXXX, Name: UNIQID3 Unique identification register 3.

Revision History		
Revision Number	Date	Tasks
V1.0	2025-12-22	Initial release of HS40J spec.
V1.1	2026-03-03	Added CW/CCW direction definition diagram Added note on magnetic reset behavior (angle-dependent turn count)